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EXAMINER

KRAIG, WILLIAM F

ART UNIT PAPER NUMBER

2815

DATE MAILED: 01/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/790,211

Applicant(s)

AOKI, TAKAAKI

Examiner

William Kraig

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 December 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 02 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3/2/04, 7/19/05
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election without traverse of claims 1-16 in the reply filed on 12/19/2005 is acknowledged.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3 and 16 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The claim to an annealing temperature being greater than 1150 is not entirely supported by the specification. The specification states that the "upper limit of the annealing temperature is, for example, 1200 (degrees) Celsius, which is the maximum temperature of the semiconductor device and the withstand temperature of the substrate". Therefore, the specification does not support a claim to an annealing temperature greater than 1200 degrees Celsius. Examiner

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believes that this claim should read --...equal to or higher than 1150 degrees Celsius and equal to or less than 1200 degrees Celsius...--, and will examine the claim as such.

3. Claims 1 and 11 rejected under 35 U.S.C. 112, 2nd paragraph, as failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The claims to forming a conductive film and a gate electrode through an insulation film are not enabled by the specification. It is unclear to the examiner, after reading the specification, how the conductive film/gate electrode are formed through the insulation film. In addition, Figs. 7-11, which describe the formation of the device, do not show a conductive film/gate electrode formed through an insulation film. From these figures, it would seem to be more accurate to describe the conductive film/gate electrode as being formed on the insulation film. Examiner recommends that the claim be amended as such, and for purposes of this office action, will examine the claims as such.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1 rejected under 35 U.S.C. 102(b) as being anticipated by Ridley et al. (U.S. Patent # 6465325).

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Regarding claim 1, Col. 4, Lines 1-50 and Figs. 2-6 of Ridley et al. disclose a method for manufacturing a semiconductor device comprising the steps of:

forming a trench (trench is area filled with insulation film (41) and conductive film (42) in Fig. 2) having an inner wall (inner wall of trench is covered with insulation film (41)) in a substrate (20, 26);

forming an insulation film (41) (Col. 4, Lines 7-8) on the inner wall of the trench;

forming a conductive film (42) (Col. 4, Lines 8-10) in the trench on the insulation film; and

annealing the substrate at an annealing temperature (Col. 4, Lines 29-39) after the step of forming the conductive film (42)

The claim to performing the annealing step for the purpose of removing a damage in the insulation film is a purely functional limitation. It is well known that similar method steps will have similar functions and effects on the final product of the method of making. Thus, as the method of Ridley et al. meets the methodological limitations of this claim, it should exhibit similar effects.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 3 rejected under 35 U.S.C. 103(a) as being unpatentable over Ridley et al. in view of Miyazaki et al. (U.S. Patent # 6258640).

Regarding claim 3, Ridley et al. discloses the method according to claim 1, wherein the substrate (20, 26) is made of silicon (Col. 3, Lines 52-55), but fails to disclose the annealing temperature being equal to or higher than 1150 degrees Celsius and equal to or less than 1200 degrees Celsius.

Miyazaki, however, teaches an RTA process wherein the annealing temperature is equal to or higher than 1150 degrees Celsius (Miyazaki, Col. 10, Lines 26-33).

It would have been obvious to one of ordinary skill in the art to incorporate the annealing temperature of Miyazaki into the process of Ridley et al. One of ordinary skill in the art would have been motivated to modify Ridley et al. in the above manner for the purpose of improving leakage characteristics of the final device (Miyazaki, Col. 10, Lines 26-33).

6. Claims 1, 5, 7, 11, and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. (U.S. Patent # 6469345) in view of Jin et al. (U.S. Patent # 6350665).

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Regarding claim 1, Aoki et al. discloses a method for manufacturing a semiconductor device comprising the steps of:

forming a trench (6) having an inner wall (inner wall of trench is covered with insulation film (7a) in Fig. 2B) in a substrate (1, 2, 3);

forming an insulation film (Fig. 2C (7a)) on the inner wall of the trench;

forming a conductive film (Fig. 2G, (8)) in the trench on the insulation film;

Aoki et al., however, fails to disclose annealing the substrate at an annealing temperature after the step of forming the conductive film so that a damage in the insulation film is removed at the annealing temperature.

Fig. 5A of Jin et al., however, teaches the annealing (524) of a substrate at an annealing temperature after the formation of a conductive gate electrode (502) (Col. 13, Lines 44-53).

It would have been obvious to one of ordinary skill in the art to incorporate the annealing step of Jin et al. into the method of Aoki et al. The ordinary artisan would have been motivated to modify the method of Aoki et al. in the above manner for the purpose of repairing damages arising from the deposition of an interlayer dielectric layer (Col. 13, Lines 44-53).

Regarding claim 5, Aoki et al. and Jin et al. disclose the method according to claim 1, wherein the conductive film is made of doped poly crystalline silicon (Aoki et al., Col. 3, Lines 7-8), and wherein the insulation film is made of silicon oxide and silicon nitride (Aoki et al., Col. 2, Lines 57-62).

Regarding claim 7, Aoki et al. and Jin et al. disclose the method according to claim 1,

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the trench (Aoki et al., Fig. 2B (6)) includes a sidewall (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)) and upper (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)) and lower portions (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) is disposed on the sidewall of the trench (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)), the upper oxide film (Aoki et al., Fig. 2H (7d)) is disposed on the upper portion of the trench (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)), and the lower oxide film (Aoki et al., Fig. 2H (7e)) is disposed on the lower portion of the trench (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) includes a silicon oxide film (Aoki et al., Fig. 2H (7a)), a silicon nitride film (Aoki et

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al., Fig. 2H (7b)) and another silicon oxide film (Aoki et al., Fig. 2H (7c)) (Aoki et al., Col. 2, Lines 57-62), and

wherein the upper (Aoki et al., Fig. 2H (7d)) and lower (Aoki et al., Fig. 2H (7e)) oxide films are made of silicon oxide (Aoki et al., Col. 2, Lines 66-67).

Regarding claim 11, Aoki et al. and Jin et al. disclose a method for manufacturing a semiconductor device comprising the steps of:

forming a trench (Aoki et al., Fig. 2H (6)) having an inner wall (Aoki et al. (inner wall of trench is covered with insulation film (7a) in Fig. 2B)) in a substrate (Aoki et al., Fig. 2H (1, 2, 3));

forming an insulation film (Aoki et al., Fig. 2H (7a, 7b, 7c)) on the inner wall of the trench;

forming a gate electrode (Aoki et al., Fig. 2H (8)) in the trench on the insulation film;

implanting an impurity into the substrate with using the gate electrode as a mask after the step of forming the gate electrode (Jin et al., Col. 10, Lines 17-25) (Jin et al., Fig. 5A (502));

performing a thermal diffusion process for diffusing the impurity so that a source region adjacent to the trench (Aoki et al., Fig. 2H (4)) and disposed on a surface of the substrate is formed (Aoki et al., Col. 3, Lines 34-38); and

annealing (Jin et al., Fig. 5A (524)) the substrate at an annealing temperature after the step of forming the conductive film (Jin et al., Fig. 5A (502))

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(Jin et al., Col. 13, Lines 44-53), so that a damage in the insulation film is removed at the annealing temperature (Jin et al., Col. 13, Lines 44-53).

Regarding claim 13, Aoki et al. and Jin et al. disclose the method according to claim 11,

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the trench (Aoki et al., Fig. 2B (6)) includes a sidewall (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)) and upper (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)) and lower portions (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) is disposed on the sidewall of the trench (Aoki et al., Fig. 2H (side walls of trench (6), having oxide film (7a) disposed thereon)), the upper oxide film (Aoki et al., Fig. 2H (7d)) is disposed on the upper portion of the trench (Aoki et al., Fig. 2H (upper portion of trench (6), having oxide film (7d) disposed thereon)), and the lower oxide film (Aoki et al., Fig. 2H (7e)) is disposed on the lower portion of the trench (Aoki et al., Fig. 2H (lower portion of trench (6), having oxide film (7e) disposed thereon)),

wherein the oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) includes a silicon oxide film (Aoki et al., Fig. 2H (7a)), a silicon nitride film (Aoki et al., Fig. 2H (7b)) and another silicon oxide film (Aoki et al., Fig. 2H (7c)) (Aoki et al., Col. 2, Lines 57-62), and

wherein the upper (Aoki et al., Fig. 2H (7d)) and lower (Aoki et al., Fig. 2H (7e)) oxide films are made of silicon oxide (Aoki et al., Col. 2, Lines 66-67).

7. Claims 2, 6, 8-10, 14, and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. in view of Jin et al., and further in view of Inagawa et al. (U.S. Patent # 6455378).

Regarding claim 2, Aoki et al. and Jin et al. disclose the method according to claim 1, further comprising the step of:

forming a source region (Aoki et al., Fig 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

Aoki et al. and Jin et al., however, fail to disclose the gate electrode including a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section, and the canopy of the gate electrode having an edge, which is disposed at a predetermined distance from an edge of an opening of the trench, and the predetermined distance being predetermined not to prevent the source region from forming.

Fig. 16(c) of Inagawa et al. teaches a gate electrode (3(3b)) including a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (See Fig. 16(c)), the canopy of the gate electrode having an edge (edge of gate electrode (3(3b)) coincident with layer (2b)), said edge being disposed at a predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) from an edge of an opening of the trench, wherein the predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) is predetermined not to prevent the source region (6) from forming (Col. 11, Lines 59-60).

It would have been obvious to one of ordinary skill in the art to incorporate the gate electrode of Inagawa et al. into the method of Aoki et al. and Jin et al. One of ordinary skill in the art would have been motivated to modify Aoki et al. and Jin et al. in

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the above manner for the purpose of having more control over the depth of the source region (Inagawa et al., Col. 11, Lines 54-60).

Regarding claim 6, Aoki et al., Jin et al., and Inagawa et al. disclose the method according to claim 5, further comprising the step of:

forming a source region (Aoki et al., Fig. 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

wherein the gate electrode (Inagawa et al., Fig. 16(c) (3(3b))) includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (Inagawa et al., Fig. 16(c)),

wherein the canopy of the gate electrode has an edge (Inagawa et al., Fig. 16(c) (edge of gate electrode (3(3b)) coincident with layer (2b))), said edge being disposed at a predetermined distance (Inagawa et al., Fig. 16(c) (distance

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between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) from an edge of an opening of the trench,

wherein the predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) is predetermined not to prevent the source region (Inagawa et al., Fig. 16(c) (6)) from forming (Inagawa et al., Col. 11, Lines 59-60).

Regarding claim 8, Aoki et al., Jin et al., and Inagawa et al. disclose the method according to claim 7, further comprising the step of:

forming a source region (Aoki et al., Fig 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

wherein the gate electrode (Inagawa et al., Fig. 16(c) (3(3b))) includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (Inagawa et al., Fig. 16(c)),

wherein the canopy of the gate electrode has an edge (Inagawa et al., Fig. 16(c) (edge of gate electrode (3(3b)) coincident with layer (2b))), said edge being

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disposed at a predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) from an edge of an opening of the trench,

wherein the predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) is predetermined not to prevent the source region (Inagawa et al., Fig. 16(c) (6)) from forming (Inagawa et al., Col. 11, Lines 59-60).

Regarding claim 9, Aoki et al., Jin et al., and Inagawa et al. disclose the method according to claim 1, wherein the device includes a cell region (Inagawa et al, Fig. 2 (area containing transistor cells (Q))) and a gate lead wire region (Inagawa et al., Fig. 2 (area containing gate line (3GL))), wherein the cell region (Inagawa et al, Fig. 2 (area containing transistor cells (Q))) includes a plurality of cells (Inagawa et al, Fig. 2 (Q)), each of which works as a transistor (Inagawa et al., Col. 6, Lines 6-14), and wherein the gate lead wire region (Inagawa et al., Fig. 2 (area containing gate line (3GL))) includes a gate lead wire (Inagawa et al, Fig. 2 (3GL)) (Inagawa et al., Col. 6, Lines 59-60).

Regarding claim 10, Aoki et al., Jin et al., and Inagawa et al. disclose the method according to claim 9, wherein the transistor (Inagawa et al, Fig. 2 (Q)) (Inagawa et al., Col. 6, Lines 6-14) is an N channel type MOSFET, a P channel type MOSFET or an IGBT (Aoki et al., Col. 2, Lines 44-47).

Regarding claim 14, Aoki et al., Jin et al., and Inagawa et al. disclose the method according to claim 13, further comprising the step of:

forming a source region (Aoki et al., Fig 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

wherein the gate electrode (Inagawa et al., Fig. 16(c) (3(3b))) includes a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (Inagawa et al., Fig. 16(c)),

wherein the canopy of the gate electrode has an edge (Inagawa et al., Fig. 16(c) (edge of gate electrode (3(3b)) coincident with layer (2b))), said edge being disposed at a predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) from an edge of an opening of the trench,

wherein the predetermined distance (Inagawa et al., Fig. 16(c) (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c)))) is predetermined not to prevent the source

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region (Inagawa et al., Fig. 16(c) (6)) from forming (Inagawa et al., Col. 11, Lines 59-60).

Regarding claim 15, Aoki et al., Jin et al., and Inagawa et al. disclose the method according to claim 14, but fail to disclose the distance between the edge of the canopy and the edge of the opening of the trench being in a range between 0.05 micrometers and 0.1 micrometers.

It would have been obvious to one of ordinary skill in the art to cause the distance between the edge of the canopy and the edge of the opening of the trench to be in a range between .05 micrometers and .1 micrometers. The claim to the specified range in the distance between the edge of the canopy and the edge of the opening on the trench constitutes an optimization of ranges. *In re Huang*, 100 F.3d 135, 40 USPQ2d 1685, 1688 (Fed. Cir. 1996)

8. Claims 3, 12, and 16 rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al., in view of Jin et al., and further in view of Miyazaki (U.S. Patent # 6258640).

Regarding claim 3, Aoki et al., and Jin et al. disclose the method according to claim 1, wherein the substrate (Aoki et al., Fig. 2H (1, 2, 3)) is made of silicon (Aoki et

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al., Col. 2, Lines 48-50), but fails to disclose the annealing temperature being equal to or higher than 1150 degrees Celsius.

Miyazaki, however, teaches an RTA process wherein the annealing temperature is equal to or higher than 1150 degrees Celsius and equal to or less than 1200 degrees Celsius (Miyazaki, Col. 10, Lines 26-33).

It would have been obvious to one of ordinary skill in the art to incorporate the annealing temperature of Miyazaki into the process of Aoki et al. and Jin et al. One of ordinary skill in the art would have been motivated to modify Aoki et al. and Jin et al. in the above manner for the purpose of improving leakage characteristics of the final device (Miyazaki, Col. 10, Lines 26-33).

Regarding claim 12, Aoki et al., Jin et al., and Miyazaki disclose the method according to claim 11, and the annealing temperature being 1150 degrees Celsius (Miyazaki, Col. 10, Lines 26-33), but fail to disclose the temperature at which the thermal diffusion process is performed or the annealing temperature in the step of annealing being higher than the process temperature in the step of performing the thermal diffusion process. The examiner takes official notice that it is well known in the art to perform thermal diffusion processes at a temperature below 1150 degrees Celsius.

Regarding claim 16, Aoki et al., Jin et al., and Miyazaki disclose the method according to claim 11, wherein the annealing temperature is equal to or higher than

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1150 degrees Celsius and equal to or less than 1200 degrees Celsius (Miyazaki, Col. 10, Lines 26-33). The examiner takes official notice that it is well known in the art to perform an annealing process in an inert gas atmosphere.

9. Claim 4 rejected under 35 U.S.C. 103(a) as being unpatentable over Aoki et al. in view of Jin et al., further in view of Miyasaki, and further in view of Inagawa et al.

Regarding claim 4, Aoki et al., Jin et al., and Miyasaki disclose the method according to claim 3, further comprising the step of:

forming a source region (Aoki et al., Fig 2B, (4)) having a contact surface between the source region and the substrate (Aoki et al., Fig. 2B, (contact surface is bottom surface of source region (4))), which is disposed near the trench (Aoki et al., Fig. 2B (6)) and is almost parallel to the substrate (see Fig. 2B),

wherein the insulation film (Aoki et al., Fig. 2C (7a)) includes an oxide-nitride-oxide film (Aoki et al., Fig. 2H (7a, 7b, 7c)) and upper (Aoki et al., Fig. 2H (7d)) and lower oxide films (Aoki et al., Fig. 2H (7e)),

wherein the conductive film (Aoki et al., Fig. 2H (8)) in the trench provides a gate electrode (Aoki et al., Col. 4, Lines 26-28),

Aoki et al., Jin et al., and Miyasaki, however, fail to disclose the gate electrode including a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section, and the canopy of the gate electrode having an edge, which is

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disposed at a predetermined distance from an edge of an opening of the trench, and the predetermined distance being predetermined not to prevent the source region from forming.

Fig. 16(c) of Inagawa et al. teaches a gate electrode (3(3b)) including a canopy for covering the upper oxide film so that the gate electrode has a T-shaped cross section (See Fig. 16(c)), the canopy of the gate electrode having an edge (edge of gate electrode (3(3b)) coincident with layer (2b)), said edge being disposed at a predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) from an edge of an opening of the trench, wherein the predetermined distance (distance between edge of gate electrode (3(3b)) coincident with layer (2b) and edge of trench opening (see Fig. 16(c))) is predetermined not to prevent the source region (6) from forming (Col. 11, Lines 59-60).

It would have been obvious to one of ordinary skill in the art to incorporate the gate electrode of Inagawa et al. into the method of Aoki et al., Jin et al., and Miyazaki. One of ordinary skill in the art would have been motivated to modify Aoki et al., Jin et al., and Miyazaki in the above manner for the purpose of having more control over the depth of the source region (Inagawa et al., Col. 11, Lines 54-60).

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**Conclusion**

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Kraig whose telephone number is 571-272-8660. The examiner can normally be reached on Mon-Fri 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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WFK

  
GEORGE ECKERT  
PRIMARY EXAMINER